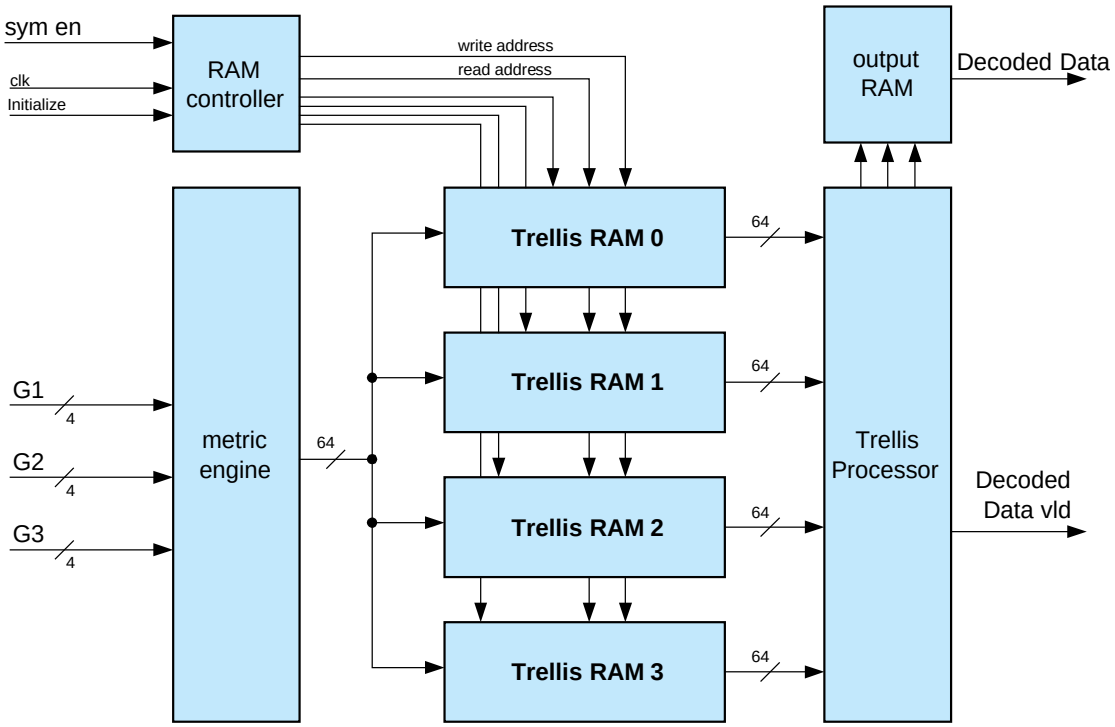
802.16-2004 Viterbi Decoder



Features

- Supports punctured modes
- 127 bit minimum traceback
- Rate ½ or 1/3 base code
- 4 bit soft decision
- Matlab Model available
- Greater than 150 M bit per sec
- Most common K=7 polynomials
- FPGA or ASIC

This Viterbi decoder is optimized for WIMAX applications, but the polynomials are general enough to support a wide range of different standards (such as DVB). The depuncturing logic and node synchronization logic is standard dependent and must be implemented external to the Viterbi decoder. The minimum traceback length is set to 127 bits, which, along with 4 bit soft decision inputs, provides close to theoretical performance for all conditions, including high puncture rates.

FPGA Resource Utilization (Altera Stratix II)

	LC Combinationals	RAM & ROM (bits)
Metric Engine	2180	0
Trellis RAMs	0	32768
Trellis Processor	385	0
Output RAM	0	256

Interface Signals

Information is applied to the Viterbi decoder one bit at a time. Three received soft decision polynomials are applied at each bit time. If one or more of the polynomials associated with the input bit are inactive, a weight of zero is associated with that input. The signal *sym_en* goes true for one clock cycle when received data for one bit is applied. This signal can be continuously valid, if new data is available at each clock cycle. There is no practical limit to the number of clock cycles of no activity separating the clock cycles with *sym_en* valid.

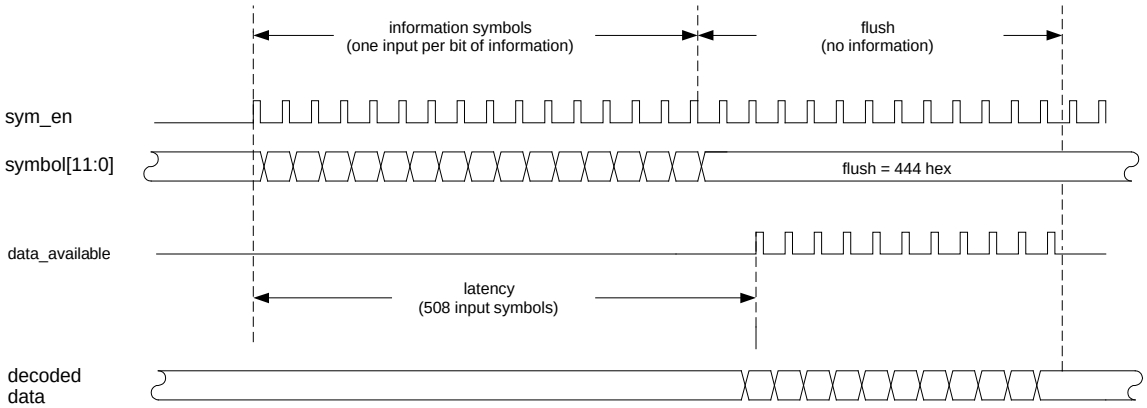
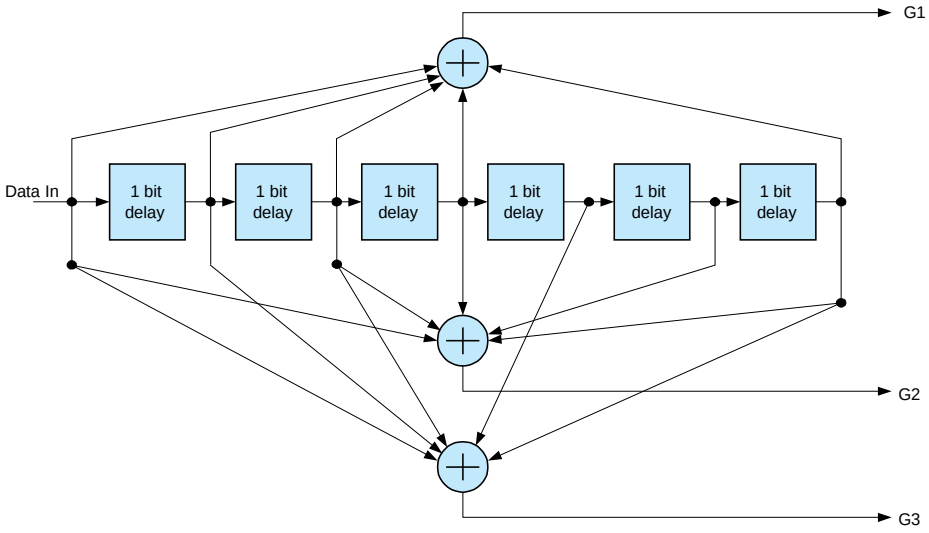


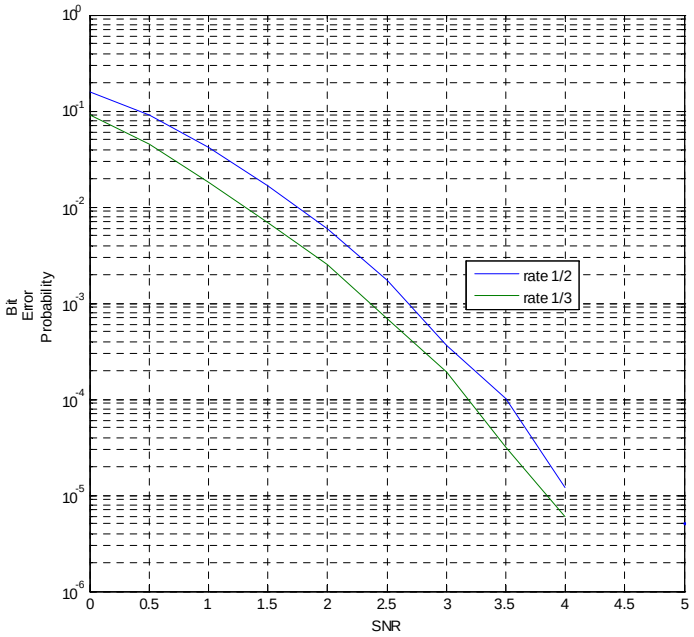
Figure 2 Top Level Timing Interfaces

The first output is presented after 508 inputs have been applied and continues to provide one output for each subsequent input. If the input is a burst, the last six bits of burst should be set to zero. After the received symbols associated with the six tail symbols have been applied to the decoder, the input should be forced to 444hex (strong zero data) and sym_en should be forced high to enable the Viterbi decoder to continue processing and providing the last 508 outputs.

Encoder


G1
Data In
1 bit delay
1 bit delay
1 bit delay
1 bit delay
1 bit delay
1 bit delay
G2
G3

Performance



Input Signals

Signal name	# of bits	Description
clk	1	Continuous square wave clock signal with a maximum frequency of 150 MHz (Stratix II)
rst	1	The decoder is initialized when this signal goes true.
sym_en	1	This signal is true each time the input code is valid.
symbol	12	Soft Decision Information Input Bits [11:8] G2 Bits [7:4] G3 Bits [3:0] G1 Any polynomial can be disabled by setting the associated input to zero (4'd0). Soft decision weighting 1000 (-8) most negative (confident ones) 1001 (-7)

		1010 (-6) 1011 (-5) 1100 (-4) 1101 (-3) 1110 (-2) 1111 (-1) 0000 (0) null 0001 (1) 0010 (2) 0011 (3) 0100 (4) 0101 (5) 0110 (6) 0111 (7) most positive (confident zeros) If the data were all ones, the encoded polynomial would be all negative numbers, and if the data were zeros, the encoded polynomial would be positive numbers.

Outputs

Signal name	# of bits	Description
Data_available	1	Goes true when the Decoded_Data output is valid.
Data_out	1	Output data.

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