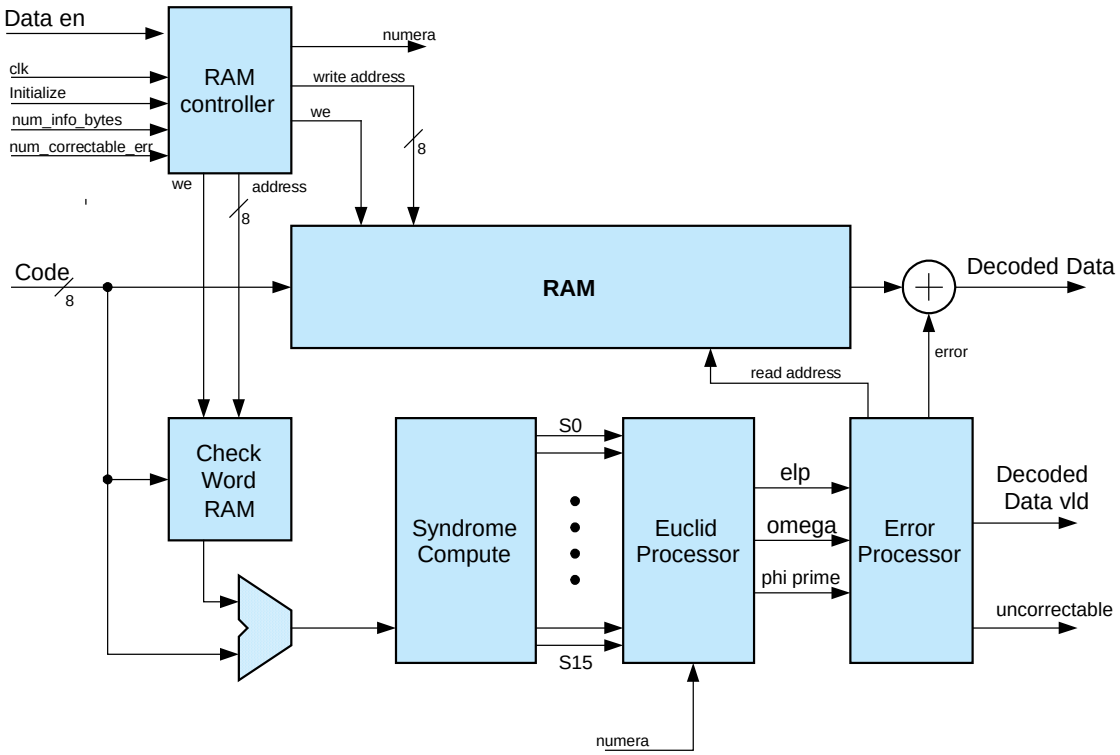
802.16-2004 Reed Solomon Decoder



Features

- Corrects 1 to 8 error words
- 1 to 239 information words
- Receives check words first
- 802.16 compliant
- Matlab Model available
- Greater than 100 M byte per sec
- Pipelined codeword processing
- FPGA or ASIC

This Reed Solomon decoder is optimized for WIMAX applications by implementing erasure capability which allows the number of corrected words to be programmed to any value from one to eight. The number of information bytes is variable from one to 239. Consistent with 802.16-2004, the check words are applied to the decoder ahead of the information words.

The decoder implements very low latency, on the order of 340 to 522 clock cycles, to simplify integration. For higher rate application, the decoder supports pipelining, where multiple code words are processed simultaneously.

FPGA Resource Utilization (Altera Stratix II)

	LC Combinationals	RAM & ROM (bits)
RAM and Controller	118	8320
Syndrome Computer	211	0
Euclid Processor	3376	0
Error Processor	1200	4096

Interface Signals

Two control signals define the mode of the Reed Solomon decoder. The *num_info_bytes* signal must have a value in the range of 1 to 239, and the *num_correctable_err* signal must be in the range of 1 to 8. The number of bytes in the code word consists of *num_info_bytes* plus two times *num_correctable_err*. The code can be applied to the decoder one byte per clock cycle, or many idle clock cycles between input words. The syndrome computation is performed as code words are written into the decoder. The Euclidian equation solver is initiated after the last code word is written to the decoder.

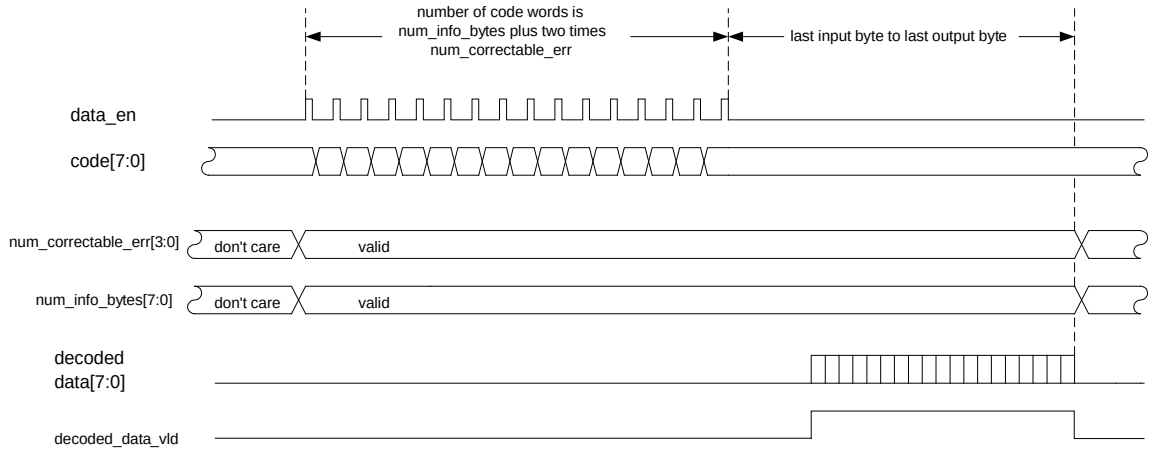


Figure 2 Top Level Timing Interfaces

When the output is available, the *decoded_data_vld* signal goes high, as the *decoded_data* output is provided one byte per clock period. The time required for processing is a function of the number of errors to be corrected.

Latency

The following table illustrates some example conditions for the decoder. The units in this table are clock cycles. The information in the last column assumes that the input is applied to the decoder in a continuous one byte per clock cycle for all check words and information words.

RS Code	Last input to last output	First input to last output
(255,239,8)	522	777
(241,239,1)	340	581
(32,24,4)	422	454
(40,36,2)	360	400
(64,48,8)	522	586
(80,72,4)	406	486
(108,96,6)	460	568
(120,108,6)	460	580

Input Signals

Signal name	# of bits	Description
clk	1	Continuous square wave clock signal with a maximum frequency of 125 MHz (Stratix II)
rst	1	The decoder is initialized when this signal goes true.
code	8	The information to be decoded is applied one byte at at time.
data_en	1	This signal is true each time the input code is valid.
num_info_bytes	8	Defines the number of information bytes
num_correctable_err	4	Defines the number of correctable errors allowed in one code word. The number of check bytes is twice this number.

Primary Outputs

Signal name	# of bits	Description
decoded_data_vld	1	Goes true when the Decoded_Data output is valid.
Decoded_data	8	Output data. The number of bytes provided by the decoder is num_info_bytes.
uncorrectable	1	Goes true if the number of errors exceeds the error correction capability of the code

Test Signal Outputs

Signal name	# of bits	Description
S1-S16	16 x8	Sixteen outputs, eight bits each, produced by the syndrome processor.
syn_state	4	State of syndrome processor. Outputs are valid when syn_state==4'd4.
numera	4	The number of correct
euclid0 –euclid16	17x8	Output of the Euclidian processor, which can assume one of these values: elp, omega or phi prime.
elp_valid	12	Goes true when Euclidian processor is providing the elp parameter.
omega_valid	12	Goes true when the Euclidian processor is providing the omega parameter.
phiprime_valid	1	Goes true when the Euclidian processor is providing the phi prime parameter.
read_address	10	Read address to the data storage RAM. The top two bits are the page, which defines which one of four blocks is being output.
error	8	The error signal produced by the error processor, which is exclusive ored with the output of the storage RAM at the locations of detected errors.

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