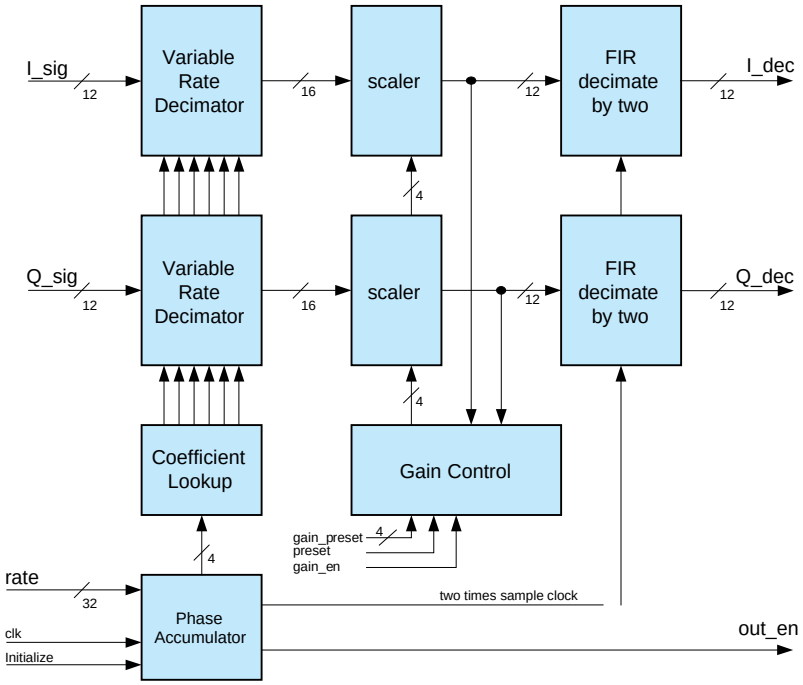
Variable Rate Decimator



Features

- 32 bit frequency precision
- 12 bit input and output precision
- Internal digital AGC
- Verilog RTL
- Matlab Model available
- Greater than 150 M bit per sec
- High adjacent channel rejection
- FPGA or ASIC

This Variable rate decimator achieves very high adjacent channel rejection by implementing two filters. The first filter provides variable rate capability and produces a signal at twice the desired sample rate. The second filter is a fixed decimate-by-two filter, and it achieves excellent rejection of out-of-band energy which is close to the desired band. The combination of the two linear phase filters produce less than one dB of in-band ripple.

The decimator can be used over a practical range of approximately 4 to 32 with 32 bits of precision in controlling the exact decimation ratio. This precision enables the decimator to be the control element of a symbol timing phase locked loop for OFDM receivers.

FPGA Resource Utilization (Altera Stratix II)

	LC Combinationals	RAM & ROM (bits)
Two Variable Rate Decimators	2232	108
Two scalers	784	0
Two Decimate-by-Two FIRs	1465	0
Phase Accumulator	133	0

Interface Signals

Figure 2 illustrates the input and output signals for the condition where the decimation rate is ¼.

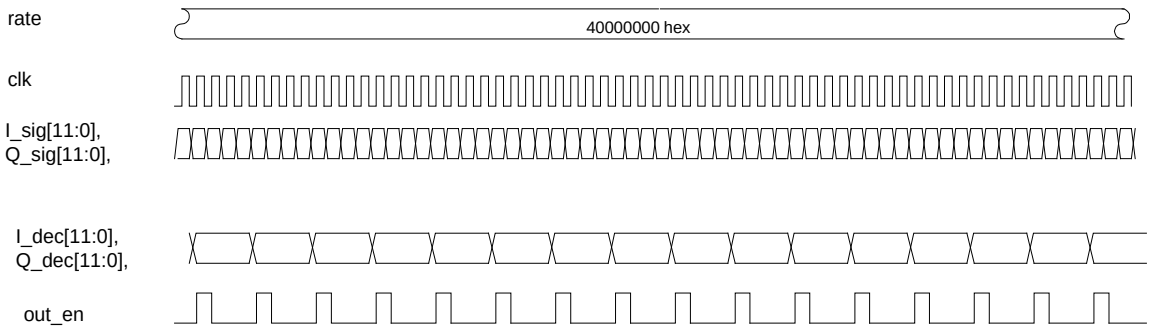


Figure 2 Top Level Timing Interfaces

AGC

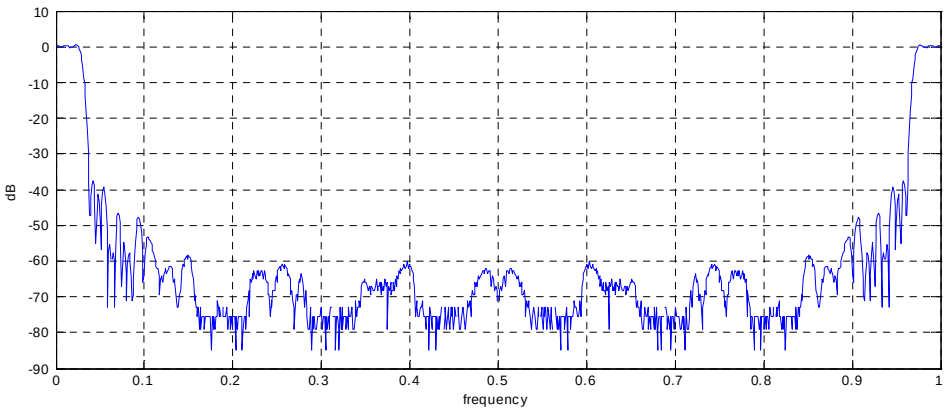
When the AGC is enabled, it attempts to control the digital gain such that the I_dec and Q_dec output signals have a median absolute value of 32. The amplitude variability has steps of 1.25 (1.9dB), 1.5 (3.5 dB), 1.75 (4.8 dB) and 2 (6 dB). The entire range is 16 steps covering 1 to 14 in amplitude (0 to 23 dB) .

In addition to the digital AGC, the RF front end must be controlled with an analog AGC which adjusts the RF gain such that the signal provided by the A/D converter is reasonably close to the desired steady state value.

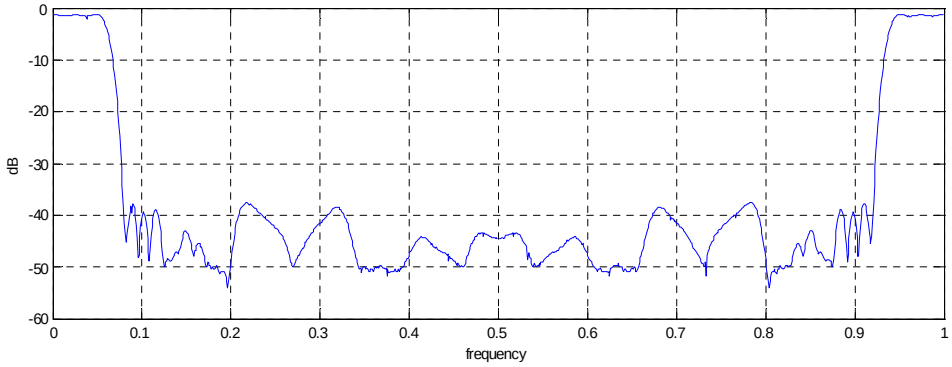
When the digital AGC is enabled, it responds with a time constant which is approximately 800 cycles of *out_en*. Once course digital AGC is achieved, it can be disabled be setting *gain_en* low, to allow signal processing to take place without steps in amplitude. Alternatively, the AGC can be disabled entirely by setting *preset* to one and controlling the gain externally via the *gain_preset* inputs.

Performance

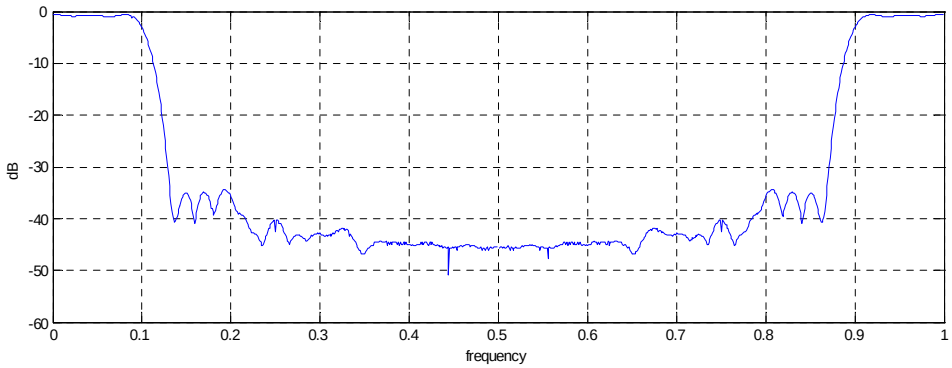
The following results assume a single sine wave input of amplitude 1000, which is swept in frequency from zero to the clock frequency. The power of the peak, absolute value at each frequency is illustrated.



Frequency response with 16:1 decimation



Frequency response with 7.5:1 decimation



Frequency response with 4.5:1 decimation

Input Signals

Signal name	# of bits	Description
clk	1	Continuous square wave clock signal with a maximum frequency of 150 MHz (Stratix II)
rst	1	The decimator is initialized when this signal goes true.
I_sig	12	Input signal in 2's complement format. One new sample is expected at each clock cycle.
Q_sig	12	Input signal in 2's complement format. One new sample is expected at each clock cycle.
rate	32	The number defines the interpolation rate, relative to the frequency of *clk*. The interpolation rate is equal to rate/2^{32}. For example, this number is set to 40000000 hex to provide an interpolation rate of ¼.
gain_en	1	This signal is set to one to enable the gain control function to update.
gain_preset	4	The intitial condition of the gain control logic.
preset	1	When this is high, the gain control logic is preset to the *gain_preset* setting in a forced, open loop manner.

Outputs

Signal name	# of bits	Description
I_dec	12	In-phase decimated output (2's complement)
Q_dec	12	Quadrature decimated output (2's complement)
out_en	1	Goes true for one clock cycle each time a new decimated output is available. The proportion of active clock cycles to total clock cycles is rate/2^{32}.

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