Digital Video
Linear Predistortion Equalizer

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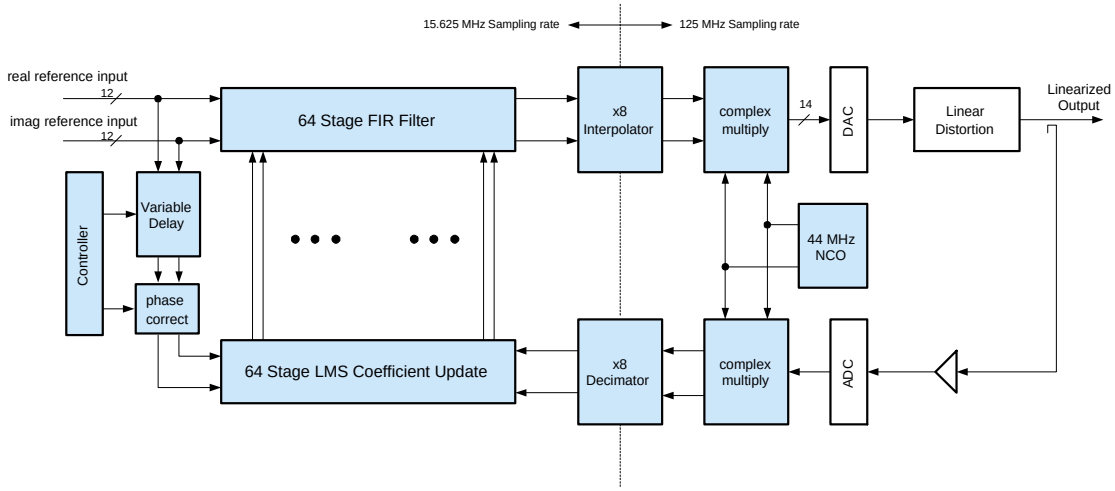

Features

- Supports 6 MHz wide television channels
- Corrects for linear distortion introduced by post HPA filtering
- Fully automatic acquisition and coefficient update
- 64 Stage equalizer covering over 4 microsecond range.
- Efficient implementation minimizes FPGA resource utilization.
- Self adaptation to a wide range of filter group delay.
- Provides predistorted IF signal at standard 44 MHz.
- Interfaces directly with the baseband signal provided by an ATSC modulator

This module is a.self adapting equalization filter, intended to compensate for linear distortion caused by the output filter in a television broadcast station. This circuit produces an intermediate frequency (IF) signal at 44 MHz center frequency, which is pre-distorted to compensate for linear distortion in the transmit chain. A sample of the transmitted signal is captured, reconverted back to 44 MHz and applied to the equalizer. The equalizer then compares the feedback sample with the desired transmit signal, and then adjusts the 64 complex coefficients of the equalizer filter to compensate for linear distortion.

Contact Mike Paff 650 941 2954 (mpaff@paffengineering.com) for more information

FPGA Resource Utilization (Altera Cyclone II)

	Logic Cells	RAM & ROM (bits)	DSP Blocks
Variable Delay	26	17920	0
Phase Compensation	32	9216	16
Equalizer Core	11373	4416	64
Decimator	663	7168	32
NCO	49	9216	0
Gain Control Logic	111	0	4
Misc.	487	0	0
Total	**12751**	**47936**	**116**

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