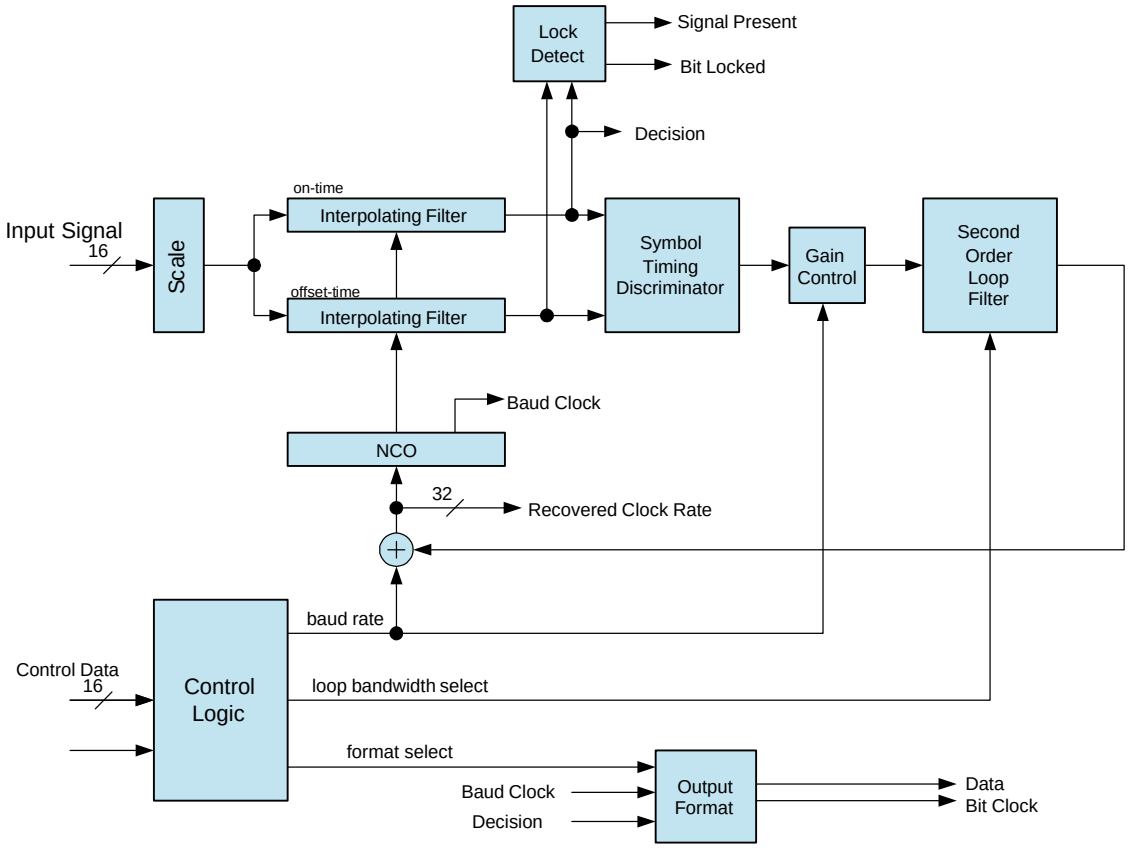
Multi-rate Bit Synchronizer

Nov. 2008



Features

- Continuously Variable Baud Rate from 100 bps to 20 M bps
- Selectable Input Format: NRZ-L, NRZ-M, NRZ-S, Bi-Phase-L, Bi-Phase-M, or Bi-Phase-S
- Fixed Rate Clock up to 120 MHz
- Verilog Source Code
- Suitable for PSK, PCM/FM, MSK, CDMA or any modulation resulting in bipolar data symbols.
- Loop Gain is independent of signal level and programmed bit rate
- Selectable Loop Bandwidth from 3% to 0.02%
- Integrate & Dump or Root Raised Cosine Matched Filter
- Output format selectable independent of input format: NRZ-L, NRZ-M, NRZ-S, Bi-Phase-L, Bi-Phase-M, or Bi-Phase-S
- Accepts up to 16 bit input data for ultra wide dynamic range

Contact Mike Paff 650 941 2954 (mpaff@paffengineering.com) for more information

This module is a digital phase locked loop, which operates at a fixed clock rate and accepts signal samples at that fixed rate, and synchronizes to the underlying binary data stream. The phase locked loop may be digitally programmed to any bit rate from 100 bits per second to 20 Mega bits per second. The loop bandwidth is programmable from a maximum of 3% of the bit rate to a minimum of less than 0.1% of the bit rate.

The acquisition range is typically three times the selected loop bandwidth, and the tracking range can be set to any practical level. This module provides hard decision outputs, but may be modified to provide soft outputs to support forward error correction.

FPGA Resource Utilization (Altera Cyclone II)

	Logic Cells	**RAM & ROM (bits)**	**DSP Blocks**
Interpolator	828	16,384	8
Loop Filter	740	0	0
Discriminator	120	0	0
Test Support	49	3072	0
Scale Logic	1291	0	8
Total	**4132**	**19456**	**16**

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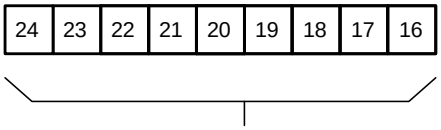
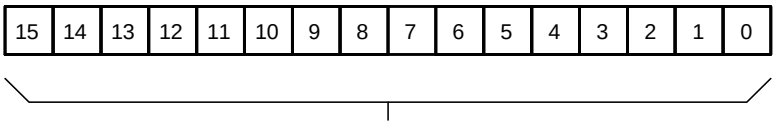
1.0 Control Information

Bit Rate Control [23:0]



bit rate:
lsb = 65,536 bps
msb = 16,777,216 bps



bit rate:
lsb = 1 bps
msb = 32768 bps

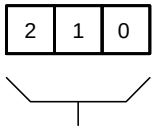
Bi Phase Mode

This input defines a bit rate in the range of 100 bits per second (bps) to 10,000,000 bits per second with a resolution of one bps. The transition rate may be as much as twice the bit rate when bi-phase modulation is used.

NRZ Mode

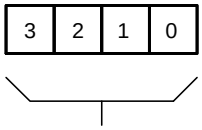
This input defines a bit rate in the range of 100 bits per second (bps) to 20,000,000 bits per second with a resolution of one bps. The transition rate is typically 50% of the bit rate in this mode, with a maximum of one phase transition per bit time.

Tracking Loop Bandwidth [2:0]



loop bandwidth:
000 0..02%
001 0.05%
010 0..09%
011 0.19%
100 0.37%
101 0.75%
110 1.5%
111 3%

Input Format [3:0]

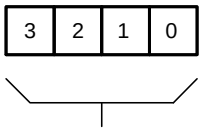


Input Encoding:
0000 NRZL
0001 NRZM
0010 NRZS
0011 Bi-PhaseL
0100 Bi-PhaseM
0101 Bi-PhaseS

Input Polarity

0: no inversion
1: input is inverted

Output Encoding



Output Encoding:
0000 NRZL
0001 NRZM
0010 NRZS
0011 Bi-PhaseL
0100 Bi-PhaseM
0101 Bi-PhaseS

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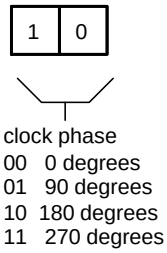
Output Polarity

0: no inversion
1: output is inverted

Output Clock Phase [1:0]



Filter Select

0: Integrate and Dump Matched Filter
1: Root Raised Cosine Filter (50% excess bandwidth)

Reset

When this input is set to one, every register in the Bit Sync is cleared to zero. This signal must be zero during normal operation

Loop Reset

The bit tracking function is reinitialized when this signal is set to a one. This signal, or Reset, must be activated following a change in Bit Rate Control, or Input Encoding or Master Clock Select.

Clock

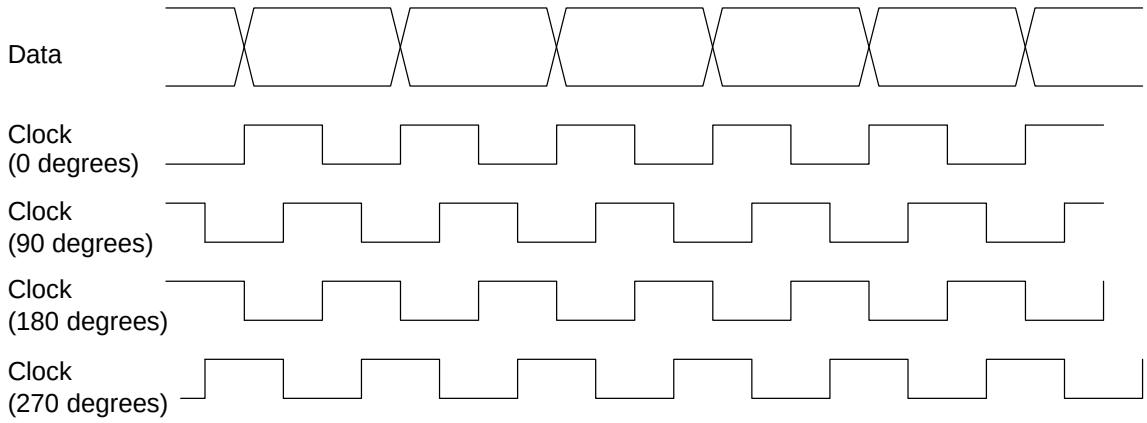
Nominal square wave of frequency 120 MHz or less.

2.0 Output Signals

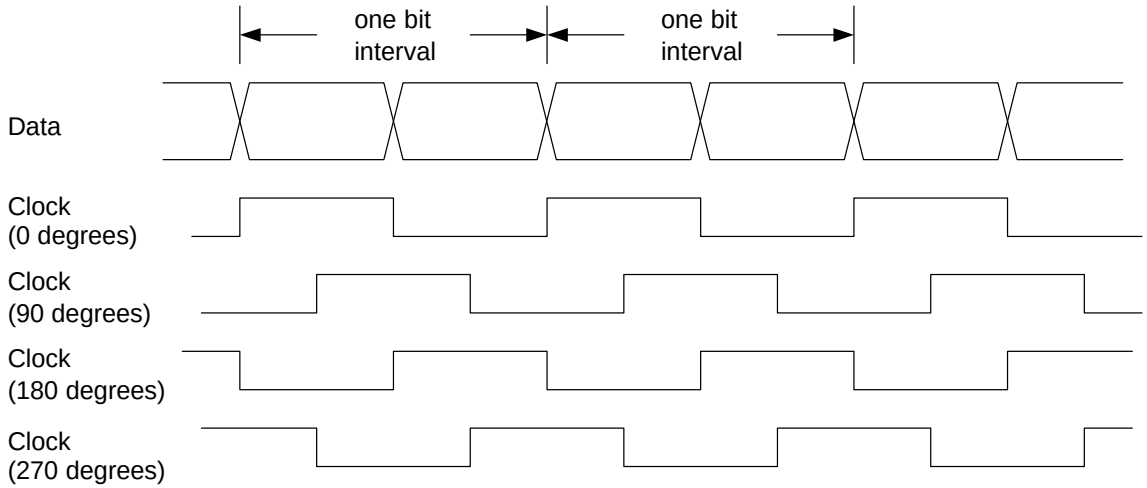
Data: Hard decision information in NRZL format. The Data is valid at the positive edge of Clock.

Clock: Nominal square wave with a frequency of the bit rate. The jitter on Clock is approximately $1/f_c$, where f_c is the selected master clock frequency.

NRZ case



Bi Phase Case



Signal Present: Goes true when transitions are detected at the input, the signal is above the minimum amplitude, and the signal is balanced between positive and negative levels.

User Selected Data: Hard decision data in the format selected by the output encoding input.

User Selected Clock: Nominal square wave with a frequency of the bit rate (even if bi-phase coding is selected).

Bit Locked: Goes true when bit timing recovery is locked.

Bit Rate [31:0]: Recovered bit rate to 32 bit resolution. The lsb has a weight of $f_c/2^{32}$. where f_c is the selected clock frequency. The recovered bit rate is given by:

$$\text{Recovered Bit Rate} = \text{Bit Rate} \times f_c / 2^{32}$$