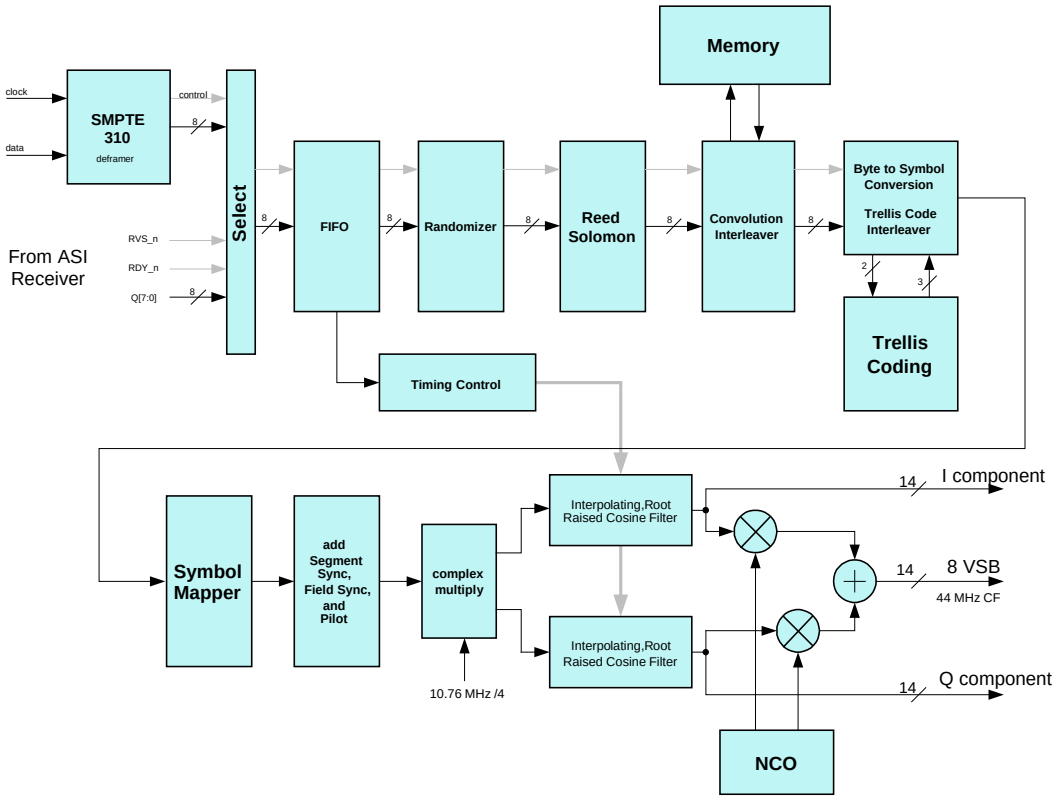
ATSC Modulator



Features

- Complies with ATSC A/53
- Supports SMPTE 310 interface
- Supports DVB-ASI interface
- Provides 44 MHz passband output
- Matlab Model available
- Symbol rate locked to transport rate
- Flexible, fixed rate clock
- FPGA or ASIC

This module receives 188 byte MPEG packets from either a SMPTE 310 source or a DVB-ASI source, and performs all functions necessary to generate an 8-VSB signal, centered at 44 MHz, and baseband components, compliant with ATSC A/53. This modulator is suitable for broadcast transmitters, ATSC test equipment or special function products which utilize a DTV interface.

Interfaces

The modulated signal produced by the transmitter has a nominal symbol rate of 10.762237 M symbols per second which carries a nominal information rate of 19.39265846 M bits per second. The exact information produced by the modulator is locked to the information rate of either the SMPTE-310 input interface or the ASI interface. The input information rate must be within 2.8 ppm of the expected nominal rate.

In the case of the SMPTE 310 interface, an equalizer and clock recovery circuit precedes the modulator. The modulator identifies the MPEG frame sync (47H), which occurs once per frame, or once every 188 bytes.

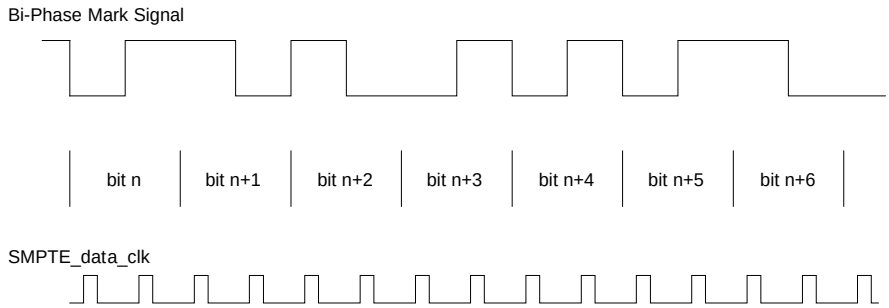


Figure 2 SMPTE 310 interface

An external chip, such as the National Semiconductor CLC016, is used to derive a clock which is synchronous to the phase transitions of the SMPTE-310 Bi-Phase Mark signal. The frequency of this clock is twice the information rate, or 38.7853169 MHz.

The DVB-ASI serial interface may be used as an alternative to the SMPTE-310. This interface operates at 270 M bits per second. Each byte of the MPEG transport stream is encoded into a ten bit serial word. The Cypress CY7B923, which is external to the modulator, receives the ASI signal and performs the 10b/8b synchronization and conversion. This chip provides parallel bytes to the modulator as illustrated in Figure 3.

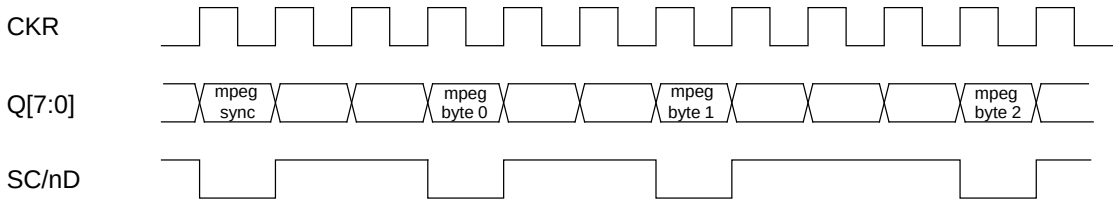


Figure 3 DVB-ASI provided by CY7B923

The byte rate of CKR provided by the CY7B923 is nominally 27 M bytes per second, which is considerably faster than the 19.39265846 M bits per second (2.4240823 M bytes per second) expected from this interface. The excess capacity of the ASI is absorbed by special characters which are transmitted as needed, and are differentiated from valid MPEG transport stream bytes. The signal SC/nD goes low when valid MPEG transport bytes are present (approximately 8.9% of the time).

Either the SMPTE-310 interface is used to provide the transport stream to the modulator, or the DVB-ASI interface, but both inputs cannot be used simultaneously. If neither input is valid, the modulator will transmit null MPEG packets.

The output passband and baseband signals are provided as 14 bit signals to drive a digital to analog converter, such as the Texas Instruments DAC904. These signals may be provided as LVDS.

Performance

The ATSC standard requires that the out-of-band emissions from the transmitter, measured in a 500 KHz band, be at least 47 dB below the total transmitted power, when measured in the 500KHz bands adjacent to the 6 MHz wide assigned band. The measured data for a signal centered at 44 MHz is approximately 7 dB better than the ATSC requirement, as shown in Figure 4.

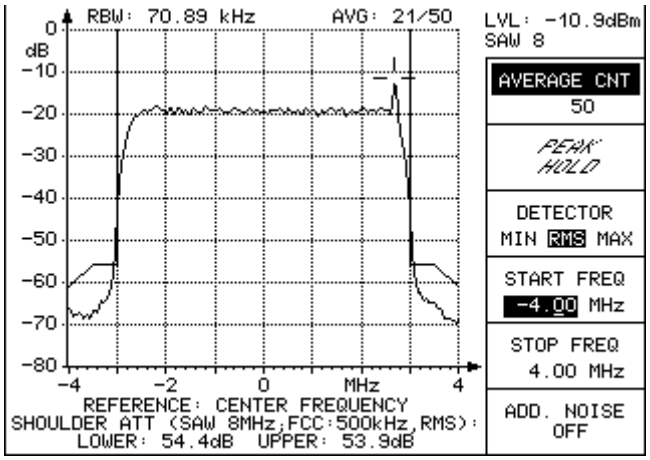


Figure 4 Measured Emission Data.

Modulation Error Ratio (MER) is a measure of the imperfections in the ATSC transmitter, and is analogous to Signal-to-Noise (SNR). The ATSC requirement for MER is 27 dB. This results in minimum loss of receiver performance (bit error rate) at

maximum range. The measured MER of this modulator is 43.6 dB, as illustrated in Figure 5.

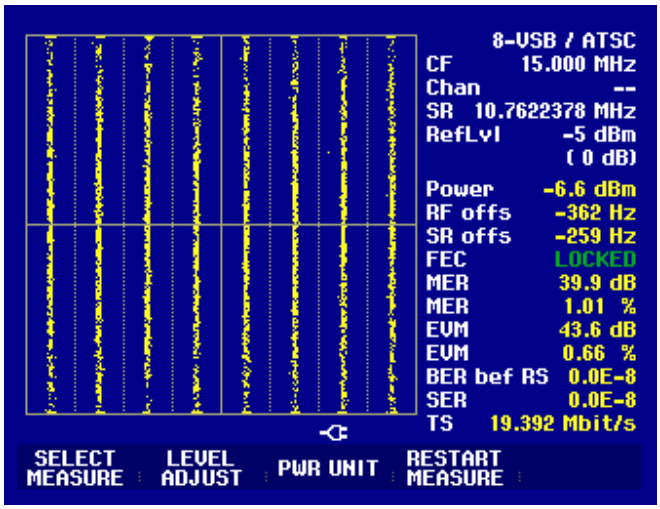


Figure 5 Measured MER and EVM

Phase noise is another potential source of performance degradation. This modulator utilizes one fixed frequency clock, which can be derived from a low phase noise crystal oscillator. Depending on system requirements, the fixed frequency clock can be anywhere in the range of 45 MHz to 125 MHz.

Altera Stratix II Resource Utilization

	ALUTs	RAM & ROM (bits)
Modulator	940	74392
Two RRC filters	4630	26880
Frequency Translation	581	18432

Altera Cyclone II Resource Utilization

	Logic Elements	RAM & ROM (bits)
Modulator	1164	77424
Two RRC filters	8070	26880
Frequency Translation	581	18432

Interface Signals

Input Signals

Signal name	# of bits	Description
clk	1	Continuous square wave clock signal with a maximum frequency of 125 MHz (Stratix II)
rst	1	The decoder is initialized when this signal goes true.
SMPTE_data_clk	1	This signal is synchronous with the phase transitions of the SMPTE-310 input, and is two times the information rate at 38.785316 MHz
SMPTE_serial_data	1	This is the Bi-phase Mark signal which is stable at the positive edge of SMPTE_data_clk
CKR	1	From CY7B923. Data transitions on the falling edge of this clock.
RVS	1	Received Violation Signal from CY7B923. This signal goes high after a code rule violation has occurred.
Q[7:0]	8	Parallel Data Output from CY7B923 which is valid at the positive edge of CKR.
SC?nD	1	Special Character signal from CY7B923. This signal is low when valid data is present.
nRDY	1	Low When receive chip is synchronized and ready to provide data.

Primary Outputs

Signal name	# of bits	Description
Passband	14	IF signal to DAC.
I_filt_sig	14	In phase baseband signal, changes synchronously with the positive transition of clk
Q_filt_sig	14	Quadrature baseband signal, changes synchronously with the positive transition of clk

Test Signal Outputs

Signal name	# of bits	Description
SMPTE_lock	1	Goes true when the SMPTE-310 interface has achieved byte sync and frame sync.
ASI_lock	1	Goes true when the ASI interface has achieved frame sync.
Field_sync	1	Goes true when field sync is transmitted every 24.197 milliseconds.
Segment_sync	1	Goes true during segment sync at a rate with a period of 77.3073 microseconds.
SMPTE_byte_clk	1	When the SMPTE-310 interface is locked, this clock will be the 2.424 MHz byte clock.

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